CY7C1470V33
CY7C1472V33
CY7C1474V33

PRELIMINARY

2M x 36/4M x 18/1M x 72 Pipelined SRAM with NoBL™ Architecture

Features

- **Zero Bus Latency™, no dead cycles between Write and Read cycles**
- **Fast clock speed: 250, 200, and 167 MHz**
- **Fast access time: 2.4, 3.0 and 3.4 ns**
- **Internally synchronized registered outputs eliminate the need to control OE**
- **Single 3.3V –5% and +5% power supply V_{DD}**
- **Separate V_{DDQ} for 3.3V or 2.5V**
- **Single WE (Read/Write) control pin**
- **Positive clock-edge triggered, address, data, and control signal registers for fully pipelined applications**
- **Interleaved or linear four-word burst capability**
- **Individual byte write ($\overline{BWS_a}$–$\overline{BWS_h}$) control (may be tied LOW)**
- **CEN pin to enable clock and suspend operations**
- **Three chip enables for simple depth expansion**
- **JTAG boundary scan for BGA packaging version**
- **Available in 119-ball bump BGA and 100-pin TQFP packages (CY7C1470V33 and CY7C1472V33).**
- **165-ball FBGA and 209-ball BGA (CY7C1474V33) package are offered by opportunity basis. (Please contact Cypress sales or marketing)**

Functional Description

The CY7C1470V33, CY7C1472V33, and CY7C1474V33 SRAMs are designed to eliminate dead cycles when making transitions from Read to Write or vice versa. These SRAMs are optimized for 100% bus utilization and achieve Zero Bus Latency. They integrate 2,097,152 × 36/4,194,304 × 18/ 1,048,576 × 72 SRAM cells, respectively, with advanced synchronous peripheral circuitry and a two-bit counter for internal burst operation. The Cypress Synchronous Burst SRAM family employs high-speed, low-power CMOS designs using advanced single-layer polysilicon, three-layer metal technology. Each memory cell consists of six transistors.

All synchronous inputs are gated by registers controlled by a positive-edge-triggered Clock Input (CLK). The synchronous inputs include all addresses, all data inputs, depth-expansion Chip Enables ($\overline{CE_1}$, CE_2, and $\overline{CE_3}$), cycle start input (ADV/$\overline{LD}$), Clock Enable ($\overline{CEN}$), Byte Write Selects ($\overline{BWS_a}$, $\overline{BWS_b}$, $\overline{BWS_c}$, $\overline{BWS_d}$, $\overline{BWS_e}$, $\overline{BWS_f}$, $\overline{BWS_g}$, $\overline{BWS_h}$), and Read/Write control ($\overline{WE}$). $\overline{BWS_c}$ and $\overline{BWS_d}$ apply to CY7C1470V33 and CY7C1472V33 only. $\overline{BWS_e}$, $\overline{BWS_f}$, $\overline{BWS_g}$, and $\overline{BWS_h}$ apply to CY7C1474V33 only.

Address and control signals are applied to the SRAM during one clock cycle, and two cycles later its associated data occurs, either Read or Write.

A Clock Enable ($\overline{CEN}$) pin allows operation of the CY7C1470V33, CY7C1472V33, and CY7C1474V33 to be suspended as long as necessary. All synchronous inputs are ignored when ($\overline{CEN}$) is HIGH; the internal device registers will hold their previous values.

There are three Chip Enable ($\overline{CE_1}$, CE_2, $\overline{CE_3}$) pins that allow the user to deselect the device when desired. If any one of these three is not active when ADV/$\overline{LD}$ is LOW, no new memory operation can be initiated and any burst cycle in progress is stopped. However, any pending data transfers (read or write) will be completed. The data bus will be in a high-impedance state two cycles after chip is deselected or a Write cycle is initiated.

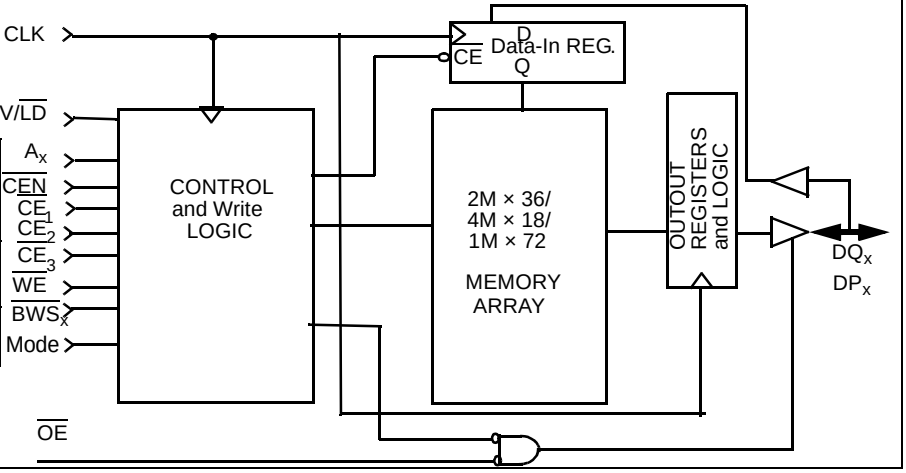
The CY7C1470V33, CY7C1472V33, and CY7C1474V33 have an on-chip two-bit burst counter. In burst mode, CY7C1470V33, CY7C1472V33, and CY7C1474V33 provide four cycles of data for a single address presented to the SRAM. The order of the burst sequence is defined by the MODE input pin. The MODE pin selects between linear and interleaved burst sequence. The ADV/$\overline{LD}$ signal is used to load a new external address (ADV/$\overline{LD}$ = LOW) or increment the internal burst counter (ADV/$\overline{LD}$ = HIGH)

Output Enable ($\overline{OE}$) and burst sequence select (MODE) are the asynchronous signals. $\overline{OE}$ can be used to disable the outputs at any given time. ZZ may be tied to LOW if it is not used.

Four pins are used to implement JTAG test capabilities. The JTAG circuitry is used to serially shift data to and from the device. JTAG inputs use LVTTL/LVCMOS levels to shift data during this testing mode of operation.

Logic Block Diagram

	A_X	DQ_X	DP_X	$\overline{BWS_X}$
2M × 36	X = 20:0	X=a,b,c,d	X=a,b,c,d	X=a,b,c,d
4M × 18	X = 21:0	X = a, b	X = a, b	X = a, b
1M × 72	X = 19:0	X = a, b, c,d,e,f,g,h	X = a, b, c,d,e,f,g,h	X = a, b c,d,e,f,g,h

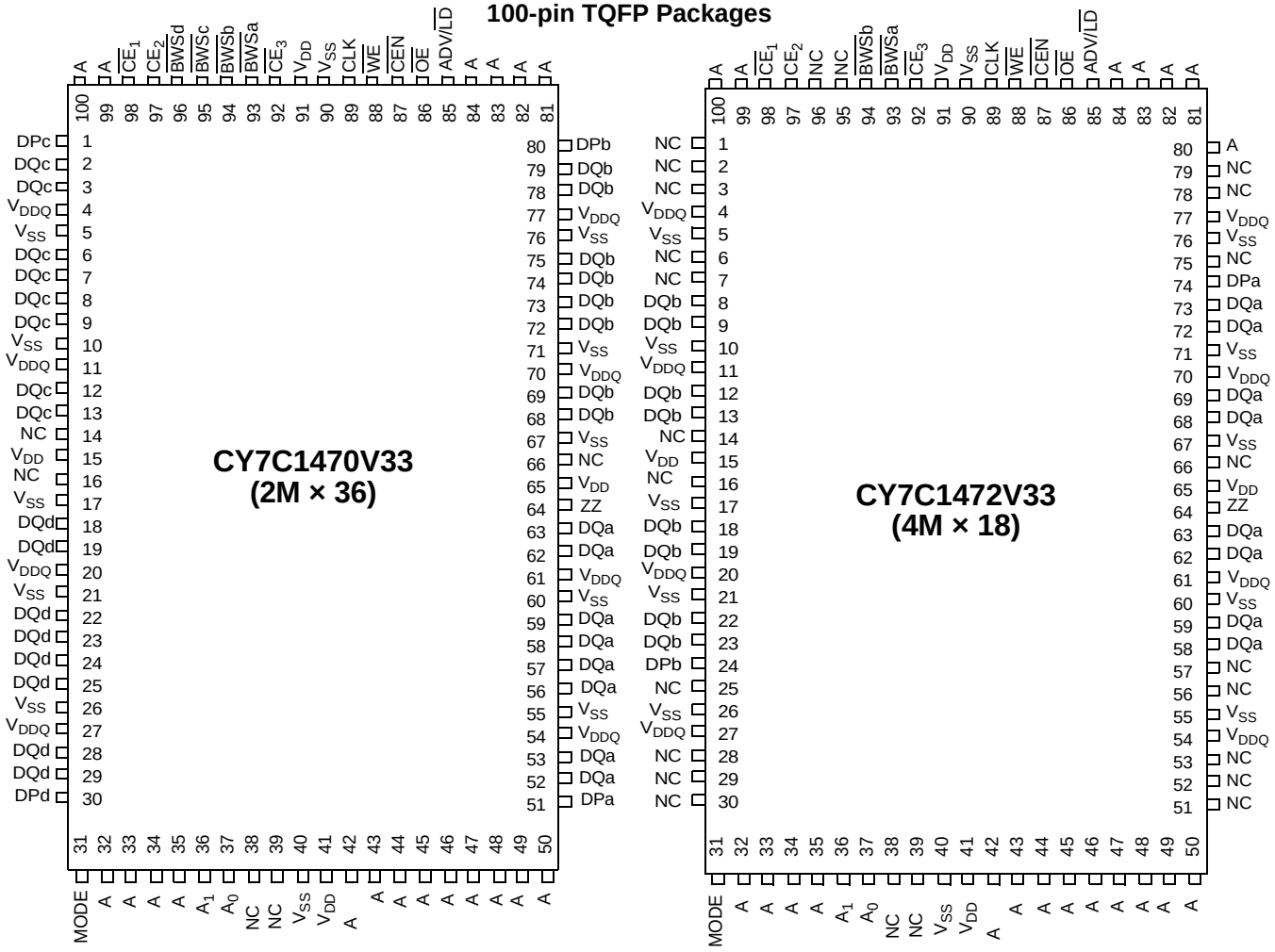


Selection Guide

	CY7C1470V33-250 CY7C1472V33-250 CY7C1474V33-250	CY7C1470V33-200 CY7C1472V33-200 CY7C1474V33-200	CY7C1470V33-167 CY7C1472V33-167 CY7C1474V33-167	Unit
Maximum Access Time	2.6	3.0	3.4	ns
Maximum Operating Current	TBD	TBD	TBD	mA
Maximum CMOS Standby Current	TBD	TBD	TBD	mA

Pin Configurations

100-pin TQFP Packages



Pin Configurations (continued)

119-ball Bump BGA
CY7C1470V33 (2M × 36)–7 × 17 BGA

	1	2	3	4	5	6	7
A	V_{DDQ}	A	A	A	A	A	V_{DDQ}
B	NC	CE_2	A	ADV/$\overline{LD}$	A	$\overline{CE_3}$	NC
C	NC	A	A	V_{DD}	A	A	NC
D	DQ_c	DP_c	V_{SS}	NC	V_{SS}	DP_b	DQ_b
E	DQ_c	DQ_c	V_{SS}	$\overline{CE_1}$	V_{SS}	DQ_b	DQ_b
F	V_{DDQ}	DQ_c	V_{SS}	$\overline{OE}$	V_{SS}	DQ_b	V_{DDQ}
G	DQ_c	DQ_c	$\overline{BWS_c}$	A	$\overline{BWS_b}$	DQ_b	DQ_b
H	DQ_c	DQ_c	V_{SS}	$\overline{WE}$	V_{SS}	DQ_b	DQ_b
J	V_{DDQ}	V_{DD}	NC	V_{DD}	NC	V_{DD}	V_{DDQ}
K	DQ_d	DQ_d	V_{SS}	CLK	V_{SS}	DQ_a	DQ_a
L	DQ_d	DQ_d	$\overline{BWS_d}$	NC	$\overline{BWS_a}$	DQ_a	DQ_a
M	V_{DDQ}	DQ_d	V_{SS}	$\overline{CEN}$	V_{SS}	DQ_a	V_{DDQ}
N	DQ_d	DQ_d	V_{SS}	A1	V_{SS}	DQ_a	DQ_a
P	DQ_d	DP_d	V_{SS}	A0	V_{SS}	DP_a	DQ_a
R	NC	A	MODE	V_{DD}	NC	A	NC
T	NC	A	A	A	A	A	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

CY7C1472V33 (4M × 18)–7 × 17 BGA

	1	2	3	4	5	6	7
A	V_{DDQ}	A	A	A	A	A	V_{DDQ}
B	NC	CE_2	A	ADV/$\overline{LD}$	A	$\overline{CE_3}$	NC
C	NC	A	A	V_{DD}	A	A	NC
D	DQ_b	NC	V_{SS}	NC	V_{SS}	DP_a	NC
E	NC	DQ_b	V_{SS}	$\overline{CE_1}$	V_{SS}	NC	DQ_a
F	V_{DDQ}	NC	V_{SS}	$\overline{OE}$	V_{SS}	DQ_a	V_{DDQ}
G	NC	DQ_b	$\overline{BWS_b}$	A	V_{SS}	NC	DQ_a
H	DQ_b	NC	V_{SS}	$\overline{WE}$	V_{SS}	DQ_a	NC
J	V_{DDQ}	V_{DD}	NC	V_{DD}	NC	V_{DD}	V_{DDQ}
K	NC	DQ_b	V_{SS}	CLK	V_{SS}	NC	DQ_a
L	DQ_b	NC	V_{SS}	NC	$\overline{BWS_a}$	DQ_a	NC
M	V_{DDQ}	DQ_b	V_{SS}	$\overline{CEN}$	V_{SS}	NC	V_{DDQ}
N	DQ_b	NC	V_{SS}	A1	V_{SS}	DQ_a	NC
P	NC	DP_b	V_{SS}	A0	V_{SS}	NC	DQ_a
R	NC	A	MODE	V_{DD}	NC	A	NC
T	A	A	A	A	A	A	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

Pin Configurations (continued)

165-ball Bump FBGA (This package is offered by opportunity basis)
CY7C1470V33 (2M × 36)–11 × 15 FBGA

	1	2	3	4	5	6	7	8	9	10	11
A	NC	A	$\overline{CE}_1$	$\overline{BWS}_c$	$\overline{BWS}_b$	$\overline{CE}_3$	$\overline{CEN}$	ADV/$\overline{LD}$	A	A	NC
B	NC	A	CE_2	$\overline{BWS}_d$	$\overline{BWS}_a$	CLK	$\overline{WE}$	$\overline{OE}$	A	A	144M
C	DPc	NC	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	DPb
D	DQc	DQc	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQb	DQb
E	DQc	DQc	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQb	DQb
F	DQc	DQc	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQb	DQb
G	DQc	DQc	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQb	DQb
H	NC	V_{DD}	NC	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	NC	NC	ZZ
J	DQd	DQd	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQa	DQa
K	DQd	DQd	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQa	DQa
L	DQd	DQd	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQa	DQa
M	DQd	DQd	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQa	DQa
N	DPd	NC	V_{DDQ}	V_{SS}	NC	NC	NC	V_{SS}	V_{DDQ}	NC	DPa
P	NC	A	A	A	TDI	A1	TDO	A	A	A	NC
R	MODE	A	A	A	TMS	A0	TCK	A	A	A	A

CY7C1472V33 (4M × 18)–11 × 15 FBGA

	1	2	3	4	5	6	7	8	9	10	11
A	NC	A	$\overline{CE}_1$	$\overline{BWS}_b$	NC	$\overline{CE}_3$	$\overline{CEN}$	ADV/$\overline{LD}$	A	A	A
B	NC	A	CE_2	NC	$\overline{BWS}_a$	CLK	$\overline{WE}$	$\overline{OE}$	A	A	144M
C	NC	NC	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	DPa
D	NC	DQb	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQa
E	NC	DQb	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQa
F	NC	DQb	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQa
G	NC	DQb	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQa
H	NC	V_{DD}	NC	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	NC	NC	ZZ
J	DQb	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQa	NC
K	DQb	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQa	NC
L	DQb	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQa	NC
M	DQb	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQa	NC
N	DPb	NC	V_{DDQ}	V_{SS}	NC	NC	NC	V_{SS}	V_{DDQ}	NC	NC
P	NC	A	A	A	TDI	A1	TDO	A	A	A	NC
R	MODE	A	A	A	TMS	A0	TCK	A	A	A	A

Pin Configurations (continued)

209-ball BGA (This package is offered by opportunity basis)
CY7C1474V33 (1M × 72)

	1	2	3	4	5	6	7	8	9	10	11
A	DQg	DQg	A	CE_2	A	ADV/$\overline{LD}$	A	$\overline{CE_3}$	A	DQb	DQb
B	DQg	DQg	$\overline{BWS_c}$	$\overline{BWS_g}$	NC	$\overline{WE}$	A	$\overline{BWS_b}$	$\overline{BWS_f}$	DQb	DQb
C	DQg	DQg	$\overline{BWS_h}$	$\overline{BWS_d}$	NC	$\overline{CE_1}$	NC	$\overline{BWS_e}$	$\overline{BWS_a}$	DQb	DQb
D	DQg	DQg	V_{SS}	NC	NC	$\overline{OE}$	NC	NC	V_{SS}	DQb	DQb
E	DPg	DPc	V_{DDQ}	V_{DDQ}	V_{DD}	V_{DD}	V_{DD}	V_{DDQ}	V_{DDQ}	DPf	DPb
F	DQc	DQc	V_{SS}	V_{SS}	V_{SS}	NC	V_{SS}	V_{SS}	V_{SS}	DQf	DQf
G	DQc	DQc	V_{DDQ}	V_{DDQ}	V_{DD}	NC	V_{DD}	V_{DDQ}	V_{DDQ}	DQf	DQf
H	DQc	DQc	V_{SS}	V_{SS}	V_{SS}	NC	V_{SS}	V_{SS}	V_{SSQ}	DQf	DQf
J	DQc	DQc	V_{DDQ}	V_{DDQ}	V_{DD}	NC	V_{DD}	V_{DDQ}	V_{DDQ}	DQf	DQf
K	NC	NC	CLK	NC	V_{SS}	$\overline{CEN}$	V_{SS}	NC	NC	NC	NC
L	DQh	DQh	V_{DDQ}	V_{DDQ}	V_{DD}	NC	V_{DD}	V_{DDQ}	V_{DDQ}	DQa	DQa
M	DQh	DQh	V_{SS}	V_{SS}	V_{SS}	NC	V_{SS}	V_{SS}	V_{SS}	DQa	DQa
N	DQh	DQh	V_{DDQ}	V_{DDQ}	V_{DD}	NC	V_{DD}	V_{DDQ}	V_{DDQ}	DQa	DQa
P	DQh	DQh	V_{SS}	V_{SS}	V_{SS}	ZZ	V_{SS}	V_{SS}	V_{SS}	DQa	DQa
R	DPd	DPh	V_{DDQ}	V_{DDQ}	V_{DD}	V_{DD}	V_{DD}	V_{DDQ}	V_{DDQ}	DPa	DPe
T	DQd	DQd	V_{SS}	NC	NC	MODE	NC	NC	V_{SS}	DQe	DQe
U	DQd	DQd	NC	A	A	A	A	A	NC	DQe	DQe
V	DQd	DQd	A	A	A	A1	A	A	A	DQe	DQe
W	DQd	DQd	TMS	TDI	A	A0	A	TDO	TCK	DQe	DQe

Pin Definitions

Pin Name	I/O Type	Pin Description
A0 A1 A	Input-Synchronous	**Address Inputs used to select one of the 2097152/4194304/1048576 address locations**. Sampled at the rising edge of the CLK.
$\overline{BWS_a}$ $\overline{BWS_b}$ $\overline{BWS_c}$ $\overline{BWS_d}$ $\overline{BWS_e}$ $\overline{BWS_f}$ $\overline{BWS_g}$ $\overline{BWS_h}$	Input-Synchronous	**Byte Write Select Inputs, active LOW**. Qualified with $\overline{WE}$ to conduct writes to the SRAM. Sampled on the rising edge of CLK. $\overline{BWS_a}$ controls DQ_a and DP_a, $\overline{BWS_b}$ controls DQ_b and DP_b, $\overline{BWS_c}$ controls DQ_c and DP_c, $\overline{BWS_d}$ controls DQ_d and DP_d. $\overline{BWS_e}$ controls DQ_e and DP_e, $\overline{BWS_f}$ controls DQ_f and DP_f, $\overline{BWS_g}$ controls DQ_g and DP_g, and $\overline{BWS_h}$ controls DQ_h and DP_h.
$\overline{WE}$	Input-Synchronous	**Write Enable Input, active LOW**. Sampled on the rising edge of CLK if $\overline{CEN}$ is active LOW. This signal must be asserted LOW to initiate a Write sequence.
ADV/$\overline{LD}$	Input-Synchronous	**Advance/load input used to advance the on-chip address counter or load a new address**. When HIGH (and $\overline{CEN}$ is asserted LOW), the internal burst counter is advanced. When LOW, a new address can be loaded into the device for an access. After being deselected, ADV/$\overline{LD}$ should be driven LOW in order to load a new address.

Pin Definitions (continued)

Pin Name	I/O Type	Pin Description
CLK	Input-Clock	**Clock Input**. Used to capture all synchronous inputs to the device. CLK is qualified with $\overline{CEN}$. CLK is only recognized if $\overline{CEN}$ is active LOW.
$\overline{CE_1}$	Input-Synchronous	**Chip Enable 1 Input, active LOW**. Sampled on the rising edge of CLK. Used in conjunction with CE_2 and $\overline{CE_3}$ to select/deselect the device.
CE_2	Input-Synchronous	**Chip Enable 2 Input, active HIGH**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE_1}$ and $\overline{CE_3}$ to select/deselect the device.
$\overline{CE_3}$	Input-Synchronous	**Chip Enable 3 Input, active LOW**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE_1}$ and CE_2 to select/deselect the device.
$\overline{OE}$	Input-Asynchronous	**Output Enable, active LOW**. Combined with the synchronous logic block inside the device to control the direction of the I/O pins. When LOW, the I/O pins are allowed to behave as outputs. When deasserted HIGH, I/O pins are three-stated, and act as input data pins. $\overline{OE}$ is masked during the data portion of a write sequence, during the first clock when emerging from a deselected state and when the device has been deselected.
$\overline{CEN}$	Input-Synchronous	**Clock Enable Input, active LOW**. When asserted LOW the clock signal is recognized by the SRAM. When deasserted HIGH the clock signal is masked. Since deasserting $\overline{CEN}$ does not deselect the device, $\overline{CEN}$ can be used to extend the previous cycle when required.
DQ_a DQ_b DQ_c DQ_d DQ_e DQ_f DQ_g DQ_h	I/O-Synchronous	**Bidirectional Data I/O Lines**. As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they deliver the data contained in the memory location specified by $A_{[x:0]}$ during the previous clock rise of the read cycle. The direction of the pins is controlled by $\overline{OE}$ and the internal control logic. When $\overline{OE}$ is asserted LOW, the pins can behave as outputs. When HIGH, DQ_a–DQ_d are placed in a three-state condition. The outputs are automatically three-stated during the data portion of a write sequence, during the first clock when emerging from a deselected state, and when the device is deselected, regardless of the state of $\overline{OE}$. DQ a, b, c, d, e, f, g, and h are eight bits wide
DP_a DP_b DP_c DP_d DP_e DP_f DP_g DP_h	I/O-Synchronous	**Bidirectional Data Parity I/O Lines**. Functionally, these signals are identical to $DQ_{[x:0]}$. DP a, b, c, d, e, f, g, and h are one bit wide.
ZZ	Input-Asynchronous	**ZZ "sleep" Input**. This active HIGH input places the device in a non-time critical "sleep" condition with data integrity preserved.
MODE	Input Strap Pin	**Mode Input**. Selects the burst order of the device. Tied HIGH selects the interleaved burst order. Pulled LOW selects the linear burst order. MODE should not change states during operation. When left floating MODE will default HIGH, to an interleaved burst order.
V_{DD}	Power Supply	**Power supply inputs to the core of the device**.
V_{DDQ}	I/O Power Supply	**Power supply for the I/O circuitry**.
V_{SS}	Ground	**Ground for the device**. Should be connected to ground of the system.
TDO	JTAG serial output Synchronous	**Serial data-out to the JTAG circuit**. Delivers data on the negative edge of TCK (BGA only).
TDI	JTAG serial input Synchronous	**Serial data-In to the JTAG circuit**. Sampled on the rising edge of TCK (BGA only).
TMS	Test Mode Select Synchronous	This **pin controls the Test Access Port state machine**. Sampled on the rising edge of TCK (BGA only).
TCK	JTAG serial clock	**Serial clock to the JTAG circuit** (BGA only).
144M	–	NC. This pin is reserved for expansion to 144 Mb.
NC	–	**No connects**.

Introduction

Functional Overview

The CY7C1470V33/CY7C1472V33/CY7C1474V33 are synchronous-pipelined Burst NoBL SRAMs designed specifically to eliminate wait states during Write/Read transitions. All synchronous inputs pass through input registers controlled by the rising edge of the clock. The clock signal is qualified with the Clock Enable input signal ($\overline{CEN}$). If $\overline{CEN}$ is HIGH, the clock signal is not recognized and all internal states are maintained. All synchronous operations are qualified with $\overline{CEN}$. All data outputs pass through output registers controlled by the rising edge of the clock. Maximum access delay from the clock rise (t_{CO}) is 2.6 ns (250-MHz device).

Accesses can be initiated by asserting Chip Enable ($\overline{CE_1}$, CE_2, $\overline{CE_3}$ on the TQFP, $\overline{CE_1}$ on the BGA) active at the rising edge of the clock. If Clock Enable ($\overline{CEN}$) is active LOW and ADV/$\overline{LD}$ is asserted LOW, the address presented to the device will be latched. The access can either be a Read or Write operation, depending on the status of the Write Enable ($\overline{WE}$). $\overline{BWS}_{[h:a]}$ can be used to conduct byte write operations.

Write operations are qualified by the Write Enable ($\overline{WE}$). All writes are simplified with on-chip synchronous self-timed write circuitry.

Synchronous Chip Enable ($\overline{CE_1}$, CE_2, $\overline{CE_3}$ on TQFP, $\overline{CE_1}$ on BGA) and an asynchronous Output Enable ($\overline{OE}$) simplify depth expansion. All operations (Reads, Writes, and Deselects) are pipelined. ADV/$\overline{LD}$ should be driven LOW once the device has been deselected in order to load a new address for the next operation.

Single Read Accesses

A read access is initiated when the following conditions are satisfied at clock rise: (1) $\overline{CEN}$ is asserted LOW, (2) chip enable asserted active, (3) the Write Enable input signal $\overline{WE}$ is deasserted HIGH, and (4) ADV/$\overline{LD}$ is asserted LOW. The address presented to the address inputs is latched into the Address Register and presented to the memory core and control logic. The control logic determines that a read access is in progress and allows the requested data to propagate to the input of the output register. At the rising edge of the next clock the requested data is allowed to propagate through the output register and onto the data bus within 2.6 ns (250-MHz device) provided $\overline{OE}$ is active LOW. After the first clock of the read access the output buffers are controlled by $\overline{OE}$ and the internal control logic. $\overline{OE}$ must be driven LOW in order for the device to drive out the requested data. During the second clock, a subsequent operation (Read/Write/Deselect) can be initiated. Deselecting the device is also pipelined. Therefore, when the SRAM is deselected at clock rise by one of the chip enable signals, its output will three-state following the next clock rise.

Burst Read Accesses

The CY7C1470V33/CY7C1472V33/CY7C1474V33 have an on-chip burst counter that allows the user the ability to supply a single address and conduct up to four Reads without reasserting the address inputs. ADV/$\overline{LD}$ must be driven LOW in order to load a new address into the SRAM, as described in the Single Read Access section above. The sequence of the burst counter is determined by the MODE input signal. A LOW input on MODE selects a linear burst mode, a HIGH selects an interleaved burst sequence. Both burst counters use A0 and A1 in the burst sequence, and will wraparound when incremented sufficiently. A HIGH input on ADV/$\overline{LD}$ will increment the internal burst counter regardless of the state of chip enable inputs or $\overline{WE}$. $\overline{WE}$ is latched at the beginning of a burst cycle. Therefore, the type of access (Read or Write) is maintained throughout the burst sequence.

Single Write Accesses

Write access are initiated when the following conditions are satisfied at clock rise: (1) $\overline{CEN}$ is asserted LOW, (2) $\overline{CE_1}$, CE_2, and $\overline{CE_3}$ are ALL asserted active, and (3) the Write signal $\overline{WE}$ is asserted LOW. The address presented to A_x is loaded into the Address Register. The write signals are latched into the Control Logic block.

On the subsequent clock rise the data lines are automatically three-stated regardless of the state of the $\overline{OE}$ input signal. This allows the external logic to present the data on DQ and DQP ($DQ_{a,b,c,d,e,f,g,h}$/$DP_{a,b,c,d,e,f,g,h}$ for CY7C1474V33, $DQ_{a,b,c,d}$/$DP_{a,b,c,d}$ for CY7C1470V33, and $DQ_{a,b}$/$DP_{a,b}$ for CY7C1472V33). In addition, the address for the subsequent access (Read/Write/Deselect) is latched into the Address Register (provided the appropriate control signals are asserted).

On the next clock rise the data presented to DQ and DP ($DQ_{a,b,c,d,e,f,g,h}$/$DP_{a,b,c,d,e,f,g,h}$ for CY7C1474V33, $DQ_{a,b,c,d}$/$DP_{a,b,c,d}$ for CY7C1470V33, and $DQ_{a,b}$/$DP_{a,b}$ for CY7C1472V33) (or a subset for byte write operations; see Write Cycle Description table for details) inputs is latched into the device and the write is complete.

The data written during the Write operation is controlled by $\overline{BWS}$ ($\overline{BWS}_{a,b,c,d,e,f,g,h}$ for CY7C1474V33, $\overline{BWS}_{a,b,c,d}$ for CY7C1470V33, and $\overline{BWS}_{a,b}$ for CY7C1472V33) signals. The CY7C1470V33/CY7C1472V33/CY7C1474V33 provides byte write capability that is described in the Write Cycle Description table. Asserting the Write Enable input ($\overline{WE}$) with the selected Byte Write Select ($\overline{BWS}$) input will selectively write only to the desired bytes. Bytes not selected during a byte write operation will remain unaltered. A Synchronous self-timed write mechanism has been provided to simplify the write operations. Byte write capability has been included in order to greatly simplify Read/Modify/Write sequences, which can be reduced to simple byte write operations.

Because the CY7C1470V33/CY7C1472V33/CY7C1474V33 is a common I/O device, data should not be driven into the device while the outputs are active. The Output Enable ($\overline{OE}$) can be deasserted HIGH before presenting data to the DQ and DP ($DQ_{a,b,c,d,e,f,g,h}$/$DP_{a,b,c,d,e,f,g,h}$ for CY7C1474V33, $DQ_{a,b,c,d}$/$DP_{a,b,c,d}$ for CY7C1470V33, and $DQ_{a,b}$/$DP_{a,b}$ for CY7C1472V33) inputs. Doing so will three-state the output drivers. As a safety precaution, DQ and DP ($DQ_{a,b,c,d,e,f,g,h}$/$DP_{a,b,c,d,e,f,g,h}$ for CY7C1474V33, $DQ_{a,b,c,d}$/$DP_{a,b,c,d}$ for CY7C1470V33, and $DQ_{a,b}$/$DP_{a,b}$ for CY7C1472V33) are automatically three-stated during the data portion of a Write cycle, regardless of the state of $\overline{OE}$.

Burst Write Accesses

The CY7C1470V33/CY7C1472V33/CY7C1474V33 has an on-chip burst counter that allows the user the ability to supply a single address and conduct up to four Write operations without reasserting the address inputs. ADV/$\overline{LD}$ must be driven LOW in order to load the initial address, as described in the Single Write Access section above. When ADV/$\overline{LD}$ is driven HIGH on the subsequent clock rise, the chip enables ($\overline{CE_1}$, CE_2, and $\overline{CE_3}$) and $\overline{WE}$ inputs are ignored and the burst counter is incremented. The correct $\overline{BWS}$ ($\overline{BWS}_{a,b,c,d,e,f,g,h}$ for CY7C1474V33, $\overline{BWS}_{a,b,c,d}$ for CY7C1470V33, and $\overline{BWS}_{a,b}$ for CY7C1472V33) inputs must be driven in each cycle of the burst write in order to write the correct bytes of data.

Cycle Description Truth Table[1, 2, 3, 4, 5, 6]

Operation	Address Used	$\overline{CE}$	$\overline{CEN}$	ADV/$\overline{LD}$/	$\overline{WE}$	$\overline{BWS_X}$	CLK	Comments
Deselected	External	1	0	0	X	X	L-H	I/Os three-state following next recognized clock.
Suspend	–	X	1	X	X	X	L-H	Clock ignored, all operations suspended.
Begin Read	External	0	0	0	1	X	L-H	Address latched.
Begin Write	External	0	0	0	0	Valid	L-H	Address latched, data presented two valid clocks later.
Burst Read Operation	Internal	X	0	1	X	X	L-H	Burst Read operation. Previous access was a Read operation. Addresses incremented internally in conjunction with the state of Mode.
Burst Write Operation	Internal	X	0	1	X	Valid	L-H	Burst Write operation. Previous access was a Write operation. Addresses incremented internally in conjunction with the state of MODE. Bytes written are determined by $\overline{BWS}_{[h:a]}$.

Interleaved Burst Sequence

First Address	Second Address	Third Address	Fourth Address
A[1:0]	A[1:0]	A[1:0]	A[1:0]
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

Linear Burst Sequence

First Address	Second Address	Third Address	Fourth Address
A[1:0]	A[1:0]	A[1:0]	A[1:0]
00	01	10	11
01	10	11	00
10	11	00	01
11	00	01	10

Sleep Mode

The ZZ input pin is an asynchronous input. Asserting ZZ places the SRAM in a power conservation “sleep” mode. Two clock cycles are required to enter into or exit from this “sleep” mode. While in this mode, data integrity is guaranteed. Accesses pending when entering the “sleep” mode are not considered valid nor is the completion of the operation guaranteed. The device must be deselected prior to entering the “sleep” mode. $\overline{CE}$s must remain inactive for the duration of t_{ZZREC} after the ZZ input returns LOW.

ZZ Mode Electrical Characteristics

Parameter	Description	Test Conditions	Min.	Max.	Unit
I_{DDZZ}	Snooze mode standby current	ZZ ≥ V_{DD} – 0.2V		15	mA
t_{ZZS}	Device operation to ZZ	ZZ ≥ V_{DD} – 0.2V		$2t_{CYC}$	ns
t_{ZZREC}	ZZ recovery time	ZZ ≤ 0.2V	$2t_{CYC}$		ns

Write Cycle Descriptions [1, 2]

Function (CY7C1470V33)	$\overline{WE}$	$\overline{BWS_d}$	$\overline{BWS_c}$	$\overline{BWS_b}$	$\overline{BWS_a}$
Read	1	X	X	X	X
Write – No Bytes Written	0	1	1	1	1
Write Byte 0 – ($DQ_{a \text{ and }} DP_{a)}$	0	1	1	1	0

Notes:
1. X =”Don't Care,” 1 = Logic HIGH, 0 = Logic LOW, $\overline{CE}$ stands for ALL Chip Enables active. $\overline{BWS}_X$ = 0 signifies at least one Byte Write Select is active, $\overline{BWS}_X$ = Valid signifies that the desired byte write selects are asserted. See Write Cycle Description table for details.
2. Write is defined by $\overline{WE}$ and $\overline{BWS}_X$. See Write Cycle Description table for details.
3. The DQ and DP pins are controlled by the current cycle and the $\overline{OE}$ signal.
4. CEN = 1 inserts wait states.
5. Device will power-up deselected and the I/Os in a three-state condition, regardless of $\overline{OE}$.
6. $\overline{OE}$ assumed LOW.

Write Cycle Descriptions (continued)[1, 2]

Function (CY7C1470V33)	$\overline{WE}$	$\overline{BWS_d}$	$\overline{BWS_c}$	$\overline{BWS_b}$	$\overline{BWS_a}$
Write Byte 1 – ($DQ_{b\ and}\ DP_{b)}$	0	1	1	0	1
Write Bytes 1, 0	0	1	1	0	0
Write Byte 2 – ($DQ_{c\ and}\ DP_{c)}$	0	1	0	1	1
Write Bytes 2, 0	0	1	0	1	0
Write Bytes 2, 1	0	1	0	0	1
Write Bytes 2, 1, 0	0	1	0	0	0
Write Byte 3 – ($DQ_{d\ and}\ DP_{d)}$	0	0	1	1	1
Write Bytes 3, 0	0	0	1	1	0
Write Bytes 3, 1	0	0	1	0	1
Write Bytes 3, 1, 0	0	0	1	0	0
Write Bytes 3, 2	0	0	0	1	1
Write Bytes 3, 2, 0	0	0	0	1	0
Write Bytes 3, 2, 1	0	0	0	0	1
Write All Bytes	0	0	0	0	0

Function (CY7C1472V33)	$\overline{WE}$	$\overline{BWS_b}$	$\overline{BWS_a}$
Read	**1**	**x**	**x**
Write – No Bytes Written	**0**	**1**	**1**
Write Byte 0 – ($DQ_{a\ and}\ DP_{a)}$	**0**	**1**	**0**
Write Byte 1 – ($DQ_{b\ and}\ DP_{b)}$	**0**	**0**	**1**
Write Both Bytes	**0**	**0**	**0**

Function (CY7C1474V33)[7]	$\overline{WE}$	$\overline{BWS_x}$
Read	**1**	**x**
Write Byte X	**0**	**0**
Write All Bytes	**0**	**All BWS = 0**

IEEE 1149.1 Serial Boundary Scan (JTAG)

The CY7C1470V33/CY7C1472V33/CY7C1474V33 incorporates a serial boundary scan Test Access Port (TAP) in the BGA package only. The TQFP package does not offer this functionality. This port operates in accordance with IEEE Standard 1149.1-1900, but does not have the set of functions required for full 1149.1 compliance. These functions from the IEEE specification are excluded because their inclusion places an added delay in the critical speed path of the SRAM. Note that the TAP controller functions in a manner that does not conflict with the operation of other devices using fully compliant 1149.1 TAPs. The TAP operates using JEDEC standard 3.3V I/O logic levels.

Disabling the JTAG Feature

It is possible to operate the SRAM without using the JTAG feature. To disable the TAP controller, TCK must be tied LOW (V_{SS}) to prevent clocking of the device. TDI and TMS are internally pulled up and may be unconnected. They may alternately be connected to V_{DD} through a pull-up resistor. TDO should be left unconnected. Upon power-up, the device will come up in a reset state which will not interfere with the operation of the device.

Test Access Port—Test Clock

The test clock is used only with the TAP controller. All inputs are captured on the rising edge of TCK. All outputs are driven from the falling edge of TCK.

Test Mode Select

The TMS input is used to give commands to the TAP controller and is sampled on the rising edge of TCK. It is allowable to leave this pin unconnected if the TAP is not used. The pin is pulled up internally, resulting in a logic HIGH level.

Note:

7. BWSx represents any byte write signal BW[0..7]. To enable any byte write BWSx, a low logic signal should be applied at clock rise. Any number of byte writes can be enabled at the same time for any given write.

Test Data-In (TDI)

The TDI pin is used to serially input information into the registers and can be connected to the input of any of the registers. The register between TDI and TDO is chosen by the instruction that is loaded into the TAP instruction register. For information on loading the instruction register, see the TAP Controller State Diagram. TDI is internally pulled up and can be unconnected if the TAP is unused in an application. TDI is connected to the Most Significant Bit (MSB) on any register.

Test Data-Out (TDO)

The TDO output pin is used to serially clock data-out from the registers. The output is active depending upon the current state of the TAP state machine (see TAP Controller State Diagram). The output changes on the falling edge of TCK. TDO is connected to the Least Significant Bit (LSB) of any register.

Performing a TAP Reset

A Reset is performed by forcing TMS HIGH (V_{DD}) for five rising edges of TCK. This RESET does not affect the operation of the SRAM and may be performed while the SRAM is operating. At power-up, the TAP is reset internally to ensure that TDO comes up in a High-Z state.

TAP Registers

Registers are connected between the TDI and TDO pins and allow data to be scanned into and out of the SRAM test circuitry. Only one register can be selected at a time through the instruction registers. Data is serially loaded into the TDI pin on the rising edge of TCK. Data is output on the TDO pin on the falling edge of TCK.

Instruction Register

Three-bit instructions can be serially loaded into the instruction register. This register is loaded when it is placed between the TDI and TDO pins as shown in the TAP Controller Block Diagram. Upon power-up, the instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a reset state as described in the previous section.

When the TAP controller is in the CaptureIR state, the two least significant bits are loaded with a binary “01” pattern to allow for fault isolation of the board level serial test path.

Bypass Register

To save time when serially shifting data through registers, it is sometimes advantageous to skip certain states. The bypass register is a single-bit register that can be placed between TDI and TDO pins. This allows data to be shifted through the SRAM with minimal delay. The bypass register is set LOW (V_{SS}) when the BYPASS instruction is executed.

Boundary Scan Register

The boundary scan register is connected to all the input and output pins on the SRAM. Several no connect (NC) pins are also included in the scan register to reserve pins for higher density devices. The ×36 configuration has a 70-bit-long register, and the ×18 configuration has a 51-bit-long register.

The boundary scan register is loaded with the contents of the RAM Input and Output ring when the TAP controller is in the Capture-DR state and is then placed between the TDI and TDO pins when the controller is moved to the Shift-DR state. The EXTEST, SAMPLE/PRELOAD and SAMPLE Z instructions can be used to capture the contents of the Input and Output ring.

The Boundary Scan Order tables show the order in which the bits are connected. Each bit corresponds to one of the bumps on the SRAM package. The MSB of the register is connected to TDI, and the LSB is connected to TDO.

Identification (ID) Register

The ID register is loaded with a vendor-specific, 32-bit code during the Capture-DR state when the IDCODE command is loaded in the instruction register. The IDCODE is hardwired into the SRAM and can be shifted out when the TAP controller is in the Shift-DR state. The ID register has a vendor code and other information described in the Identification Register Definitions table.

TAP Instruction Set

Eight different instructions are possible with the three-bit instruction register. All combinations are listed in the Instruction Code table. Three of these instructions are listed as RESERVED and should not be used. The other five instructions are described in detail below.

The TAP controller used in this SRAM is not fully compliant with the 1149.1 convention because some of the mandatory 1149.1 instructions are not fully implemented. The TAP controller cannot be used to load address, data, or control signals into the SRAM and cannot preload the Input or Output buffers. The SRAM does not implement the 1149.1 commands EXTEST or INTEST or the PRELOAD portion of SAMPLE/PRELOAD; rather it performs a capture of the Inputs and Output ring when these instructions are executed.

Instructions are loaded into the TAP controller during the Shift-IR state when the instruction register is placed between TDI and TDO. During this state, instructions are shifted through the instruction register through the TDI and TDO pins. To execute the instruction once it is shifted in, the TAP controller needs to be moved into the Update-IR state.

EXTEST

EXTEST is a mandatory 1149.1 instruction that is to be executed whenever the instruction register is loaded with all 0s. EXTEST is not implemented in the TAP controller, and therefore this device is not compliant with the 1149.1 standard.

The TAP controller does recognize an all-0 instruction. When an EXTEST instruction is loaded into the instruction register, the SRAM responds as if a SAMPLE/PRELOAD instruction has been loaded. There is one difference between the two instructions. Unlike the SAMPLE/PRELOAD instruction, EXTEST places the SRAM outputs in a High-Z state.

IDCODE

The IDCODE instruction causes a vendor-specific, 32-bit code to be loaded into the instruction register. It also places the instruction register between the TDI and TDO pins and allows the IDCODE to be shifted out of the device when the TAP controller enters the Shift-DR state. The IDCODE instruction is loaded into the instruction register upon power-up or whenever the TAP controller is given a test logic reset state.

SAMPLE Z

The SAMPLE Z instruction causes the boundary scan register to be connected between the TDI and TDO pins when the TAP controller is in a Shift-DR state. It also places all SRAM outputs into a High-Z state.

SAMPLE/PRELOAD

SAMPLE/PRELOAD is a 1149.1 mandatory instruction. The PRELOAD portion of this instruction is not implemented, so the TAP controller is not fully 1149.1-compliant.

When the SAMPLE/PRELOAD instructions are loaded into the instruction register and the TAP controller is in the Capture-DR state, a snapshot of data on the inputs and output pins is captured in the boundary scan register.

The user must be aware that the TAP controller clock can only operate at a frequency up to 10 MHz, while the SRAM clock operates more than an order of magnitude faster. Because there is a large difference in the clock frequencies, it is possible that during the Capture-DR state, an input or output will undergo a transition. The TAP may then try to capture a signal while in transition (metastable state). This will not harm the device, but there is no guarantee as to the value that will be captured. Repeatable results may not be possible.

To guarantee that the boundary scan register will capture the correct value of a signal, the SRAM signal must be stabilized long enough to meet the TAP controller's capture set-up plus hold times (t_{CS} and t_{CH}). The SRAM clock input might not be captured correctly if there is no way in a design to stop (or slow) the clock during a SAMPLE/PRELOAD instruction. If this is an issue, it is still possible to capture all other signals and simply ignore the value of the CK and CK# captured in the boundary scan register.

Once the data is captured, it is possible to shift out the data by putting the TAP into the Shift-DR state. This places the boundary scan register between the TDI and TDO pins.

Note that since the PRELOAD part of the command is not implemented, putting the TAP into the Update to the Update-DR state while performing a SAMPLE/PRELOAD instruction will have the same effect as the Pause-DR command.

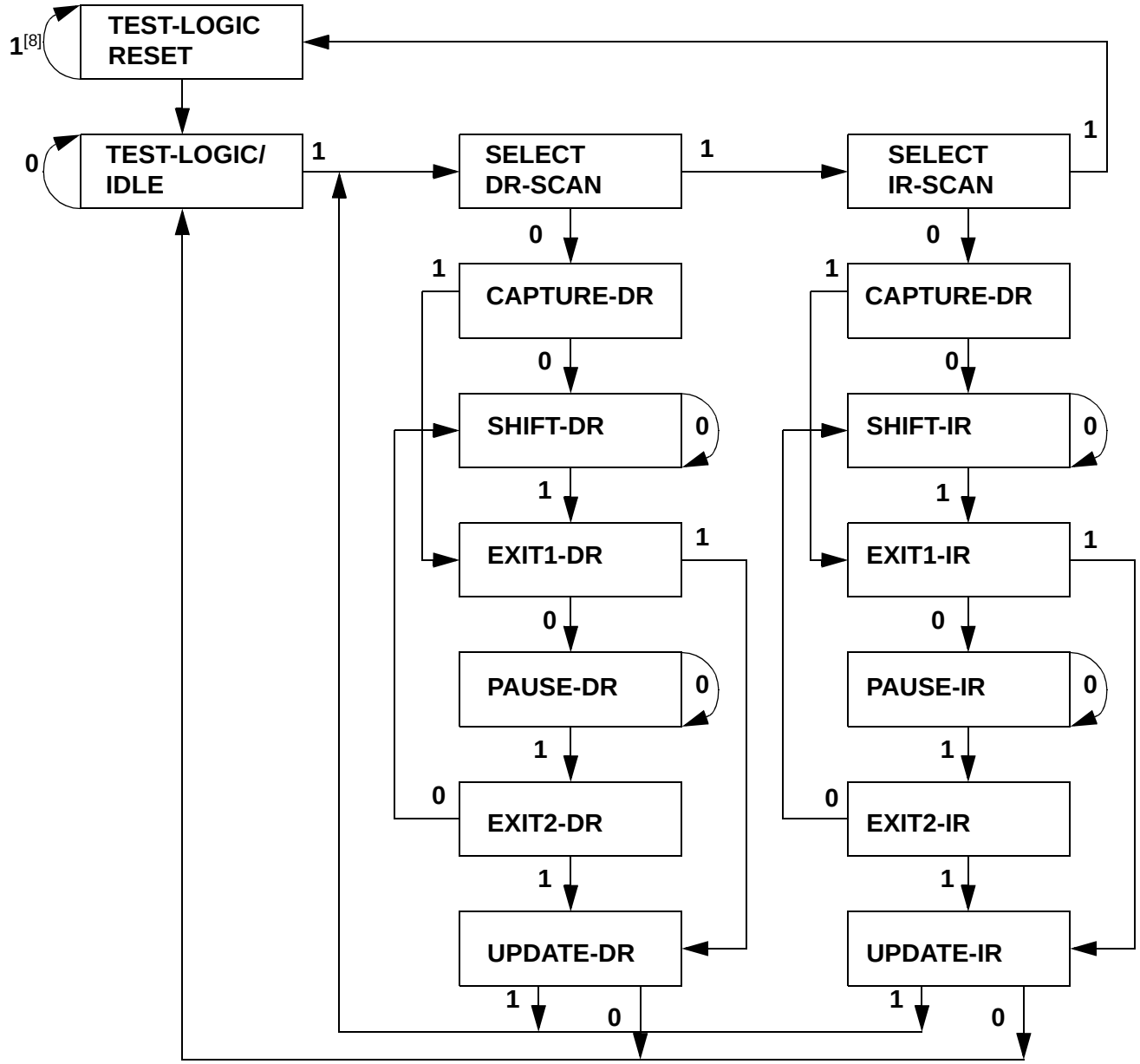
Bypass

When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a Shift-DR state, the bypass register is placed between the TDI and TDO pins. The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board.

Reserved

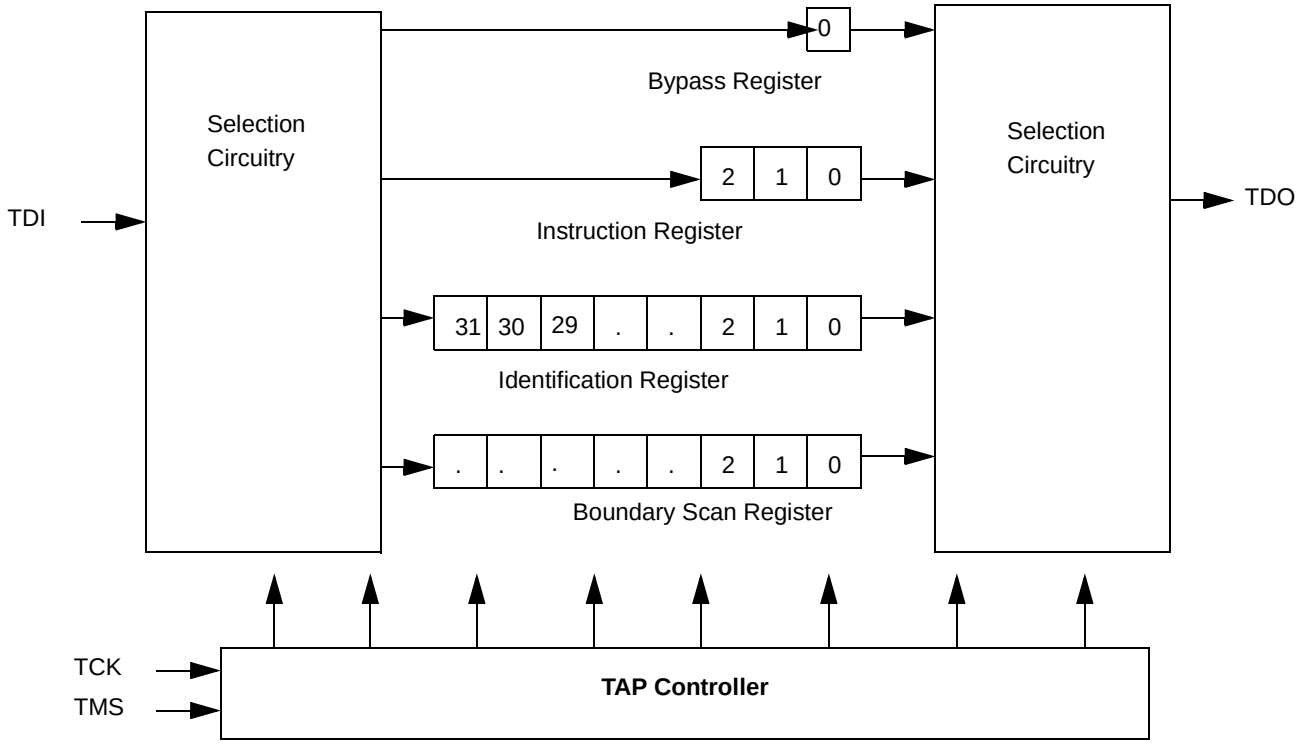
These instructions are not implemented but are reserved for future use. Do not use these instructions.

TAP Controller State Diagram



Note:
8. The 0/1 next to each state represents the value at TMS at the rising edge of TCK.

TAP Controller Block Diagram



TAP Electrical Characteristics Over the Operating Range[9, 10]

Parameter	Description	Test Conditions	Min.	Max.	Unit
V_{OH1}	Output HIGH Voltage	I_{OH} = –4.0 mA	2.4		V
V_{OH2}	Output HIGH Voltage	I_{OH} = –100 µA	3.0		V
V_{OL1}	Output LOW Voltage	I_{OL} = 8.0 mA		0.4	V
V_{OL2}	Output LOW Voltage	I_{OL} = 100 µA		0.2	V
V_{IH}	Input HIGH Voltage		1.8	V_{DD} + 0.3	V
V_{IL}	Input LOW Voltage		–0.5	0.8	V
I_X	Input Load Current	GND ≤ V_I ≤ V_{DDQ}	–5	5	µA

TAP AC Switching Characteristics Over the Operating Range [11, 12]

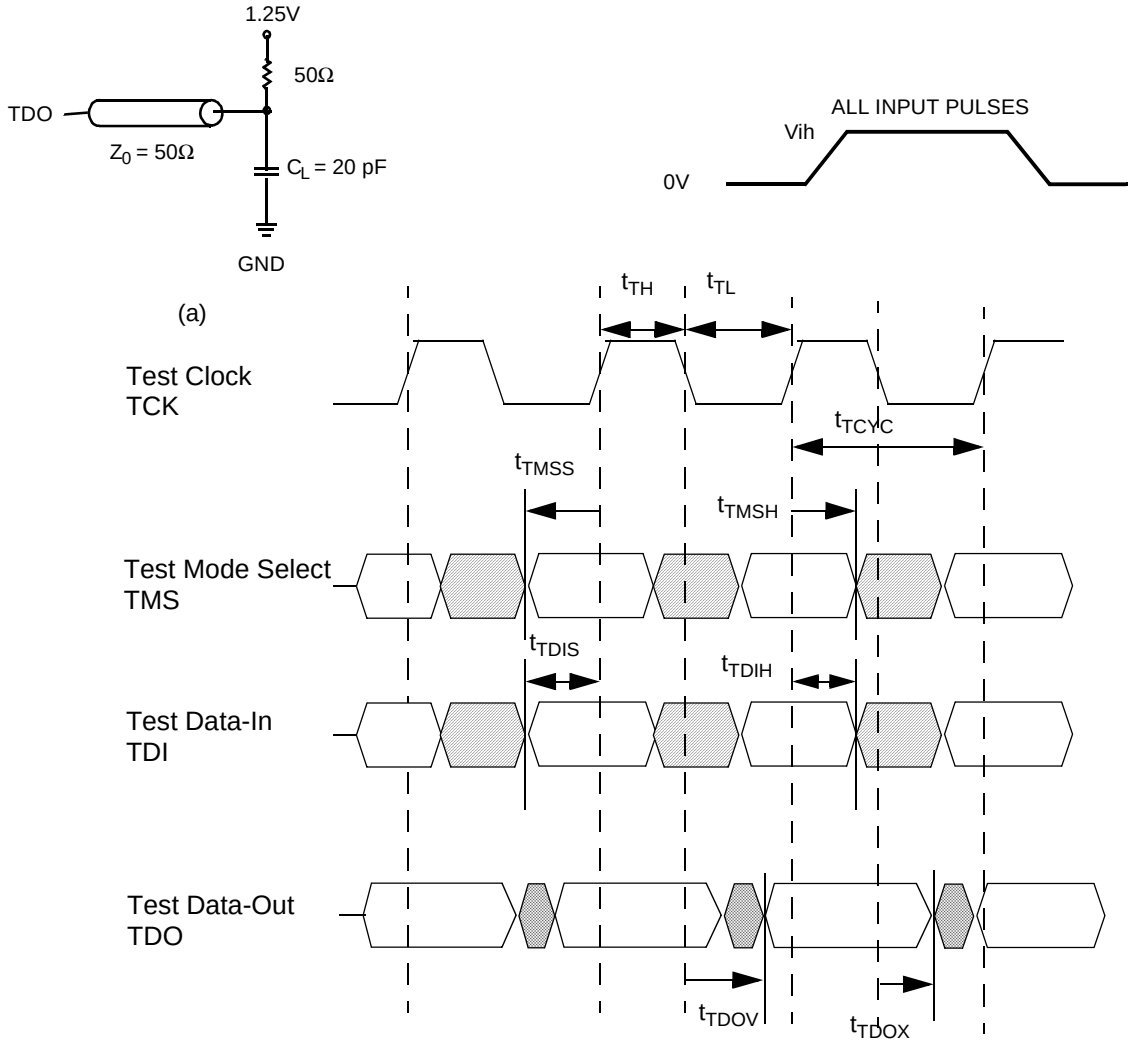
Parameter	Description	Min.	Max.	Unit
t_{TCYC}	TCK Clock Cycle Time	100		ns
t_{TF}	TCK Clock Frequency		10	MHz
t_{TH}	TCK Clock HIGH	40		ns
t_{TL}	TCK Clock LOW	40		ns
Set-up Times				
t_{TMSS}	TMS Set-up to TCK Clock Rise	10		ns
t_{TDIS}	TDI Set-up to TCK Clock Rise	10		ns
t_{CS}	Capture Set-up to TCK Rise	10		ns

Notes:
9. All voltage referenced to Ground.
10. Overshoot: $V_{IH}(AC) \le V_{DD} + 1.5V$ for $t \le t_{TCYC}/2$; undershoot: $V_{IL}(AC) \le 0.5V$ for $t \le t_{TCYC}/2$; power-up: $V_{IH} < 2.6V$ and $V_{DD} < 2.4V$ and $V_{DDQ} < 1.4V$ for $t < 200$ ms.
11. t_{CS} and t_{CH} refer to the set-up and hold time requirements of latching data from the boundary scan register.
12. Test conditions are specified using the load in TAP AC test conditions. t_R/t_F = 1 ns.

TAP AC Switching Characteristics Over the Operating Range (continued)[11, 12]

Parameter	Description	Min.	Max.	Unit
Hold Times				
t_{TMSH}	TMS Hold after TCK Clock Rise	10		ns
t_{TDIH}	TDI Hold after Clock Rise	10		ns
t_{CH}	Capture Hold after Clock Rise	10		ns
Output Times				
t_{TDOV}	TCK Clock LOW to TDO Valid		20	ns
t_{TDOX}	TCK Clock LOW to TDO Invalid	0		ns

TAP Timing and Test Conditions



Identification Register Definitions

Instruction Field	×18	×36	X72	Description
Revision Number (31:29)	000	000	000	Reserved for version number
Department Number (27:25)	101	101	101	Department number
Voltage (28&24)	00	00	00	
Architecture (23:21)	001	001	001	Architecture type
Memory type (20:18)	000	000	000	Defines type of memory
Device Width (17:15)	010	100	110	Defines width of the SRAM. ×36 or ×18
Device Density (14:12)	100	100	100	Defines the density of the SRAM
Cypress JEDEC ID (11:1)	00000110100	00000110100	00000110100	Allows unique identification of SRAM vendor
ID Register Presence (0)	1	1	1	Indicate the presence of an ID register.

Scan Register Sizes

Register Name	Bit Size (x18)	Bit Size (x36)	Bit Size (x72)
Instruction	3	3	3
Bypass	1	1	1
ID	32	32	32
Boundary Scan	TBD	TBD	TBD

Identification Codes

Instruction	Code	Description
EXTEST	000	Captures the Input/Output ring contents. Places the boundary scan register between the TDI and TDO. Forces all SRAM outputs to High-Z state. This instruction is not 1149.1-compliant.
IDCODE	001	Loads the ID register with the vendor ID code and places the register between TDI and TDO. This operation does not affect SRAM operation.
SAMPLE Z	010	Captures the Input/Output contents. Places the boundary scan register between TDI and TDO. Forces all SRAM output drivers to a High-Z state.
RESERVED	011	Do Not Use. This instruction is reserved for future use.
SAMPLE/PRELOAD	100	Captures the Input/Output ring contents. Places the boundary scan register between TDI and TDO. Does not affect the SRAM operation. This instruction does not implement 1149.1 preload function and is therefore not 1149.1-compliant.
RESERVED	101	Do Not Use. This instruction is reserved for future use.
RESERVED	110	Do Not Use. This instruction is reserved for future use.
BYPASS	111	Places the bypass register between TDI and TDO. This operation does not affect SRAM operation.

Boundary Scan Order (2M × 36)

TBD	TBD	TBD	TBD	TBD	TBD
TBD	TBD	TBD	TBD	TBD	TBD
TBD	TBD	TBD	TBD	TBD	TBD
TBD	TBD	TBD	TBD	TBD	TBD
TBD	TBD	TBD	TBD	TBD	TBD
TBD	TBD	TBD	TBD	TBD	TBD
TBD	TBD	TBD	TBD	TBD	TBD
TBD	TBD	TBD	TBD	TBD	TBD
TBD	TBD	TBD	TBD	TBD	TBD
TBD	TBD	TBD	TBD	TBD	TBD
TBD	TBD	TBD	TBD	TBD	TBD
TBD	TBD	TBD	TBD	TBD	TBD
TBD	TBD	TBD	TBD	TBD	TBD
TBD	TBD	TBD	TBD	TBD	TBD
TBD	TBD	TBD	TBD	TBD	TBD
TBD	TBD	TBD	TBD	TBD	TBD
TBD	TBD	TBD	TBD	TBD	TBD
TBD	TBD	TBD	TBD	TBD	TBD
TBD	TBD	TBD	TBD	TBD	TBD
TBD	TBD	TBD	TBD	TBD	TBD
TBD	TBD	TBD	TBD	TBD	TBD
TBD	TBD	TBD	TBD	TBD	TBD
TBD	TBD	TBD	TBD	TBD	TBD
TBD	TBD	TBD	TBD	TBD	TBD
TBD	TBD	TBD	TBD	TBD	TBD
TBD	TBD	TBD	TBD	TBD	TBD
TBD	TBD	TBD	TBD	TBD	TBD
TBD	TBD	TBD	TBD	TBD	TBD
TBD	TBD	TBD	TBD	TBD	TBD
TBD	TBD	TBD	TBD	TBD	TBD
TBD	TBD	TBD	TBD	TBD	TBD
TBD	TBD	TBD	TBD	TBD	TBD
TBD	TBD	TBD	TBD	TBD	TBD
TBD	TBD	TBD	TBD	TBD	TBD
TBD	TBD	TBD	TBD	TBD	TBD
TBD	TBD	TBD	TBD	TBD	TBD
TBD	TBD	TBD	TBD	TBD	TBD
TBD	TBD	TBD	TBD	TBD	TBD
TBD	TBD	TBD	TBD	TBD	TBD

Boundary Scan Order (4M × 18)

TBD	TBD	TBD	TBD	TBD	TBD
TBD	TBD	TBD	TBD	TBD	TBD
TBD	TBD	TBD	TBD	TBD	TBD
TBD	TBD	TBD	TBD	TBD	TBD
TBD	TBD	TBD	TBD	TBD	TBD
TBD	TBD	TBD	TBD	TBD	TBD
TBD	TBD	TBD	TBD	TBD	TBD
TBD	TBD	TBD	TBD	TBD	TBD
TBD	TBD	TBD	TBD	TBD	TBD
TBD	TBD	TBD	TBD	TBD	TBD
TBD	TBD	TBD	TBD	TBD	TBD
TBD	TBD	TBD	TBD	TBD	TBD
TBD	TBD	TBD	TBD	TBD	TBD
TBD	TBD	TBD	TBD	TBD	TBD
TBD	TBD	TBD	TBD	TBD	TBD
TBD	TBD	TBD	TBD	TBD	TBD
TBD	TBD	TBD	TBD	TBD	TBD
TBD	TBD	TBD	TBD	TBD	TBD
TBD	TBD	TBD	TBD	TBD	TBD
TBD	TBD	TBD	TBD	TBD	TBD
TBD	TBD	TBD	TBD	TBD	TBD
TBD	TBD	TBD	TBD	TBD	TBD
TBD	TBD	TBD	TBD	TBD	TBD
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TBD	TBD	TBD	TBD	TBD	TBD
TBD	TBD	TBD	TBD	TBD	TBD
TBD	TBD	TBD	TBD	TBD	TBD

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....–65°C to +150°C

Ambient Temperature with Power Applied.....–55°C to +125°C

Supply Voltage on V_{DD} Relative to GND.....–0.5V to +4.6V

DC Voltage Applied to Outputs in High-Z State[14] ..... –0.5V to V_{DDQ} + 0.5V

DC Input Voltage[14] ..... –0.5V to V_{DDQ} + 0.5V

Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage..... > 2001V (per MIL-STD-883, Method 3015)

Latch-up Current..... > 200 mA

Operating Range

Range	Ambient Temperature[13]	V_{DD}	V_{DDQ}
Com'l	0°C to +70°C	3.3V ±5%	2.375V (min.) V_{DD} (max)

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Max.	Unit
V_{DD}	Power Supply Voltage			3.135	3.465	V
V_{DDQ}	I/O Supply Voltage			2.375	V_{DD}	V
V_{OH}	Output HIGH Voltage	V_{DD} = Min., I_{OH} = –4.0 mA	3.3V	2.4		V
		V_{DD} = Min., I_{OH} = –1.0 mA	2.5V	2.0		V
V_{OL}	Output LOW Voltage	V_{DD} = Min., I_{OL} = 8.0 mA	3.3V		0.4	V
		V_{DD} = Min., I_{OL} = 1.0 mA	2.5V		0.4	V
V_{IH}	Input HIGH Voltage		3.3 V	2.0		V
			2.5V	1.7		V
V_{IL}	Input LOW Voltage[14]		3.3V	–0.3	0.8	V
			2.5V	–0.3	0.7	V
I_X	Input Load Current	GND ≤ V_I ≤ V_{DDQ}			5	µA
	Input Current of MODE				30	µA
	Input Current of ZZ	Input = V_{SS}			30	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{DDQ}, Output Disabled			5	µA
I_{DD}	V_{DD} Operating Supply	V_{DD} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{CYC}$	250 MHz		TBD	mA
			200 MHz		TBD	mA
			167 MHz		TBD	mA
I_{SB1}	Automatic CE Power-down Current—TTL Inputs	Max. V_{DD}, Device Deselected, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL} f = f_{MAX} = $1/t_{CYC}$	250 MHz		TBD	mA
			200 MHz		TBD	mA
			167 MHz		TBD	mA
I_{SB2}	Automatic CE Power-down Current—CMOS Inputs	Max. V_{DD}, Device Deselected, V_{IN} ≤ 0.3V or V_{IN} ≥ V_{DDQ} − 0.3V, f = 0	All speed grades		TBD	mA
I_{SB3}	Automatic CE Power-down Current—CMOS Inputs	Max. V_{DD}, Device Deselected, or V_{IN} ≤ 0.3V or V_{IN} ≥ V_{DDQ} − 0.3V f = f_{MAX} = $1/t_{CYC}$	250 MHz		TBD	mA
			200 MHz		TBD	mA
			167 MHz		TBD	mA
I_{SB4}	Automatic CE Power-down Current—TTL Inputs	Max. V_{DD}, Device Deselected, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = 0	All speed grades		TBD	mA

Shaded areas contain advance information.

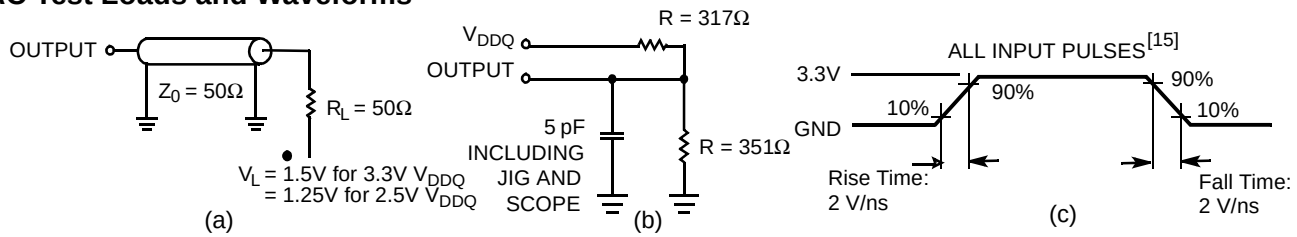
Notes:

13. T_A is the ambient temperature.
14. Minimum voltage equals –2.0V for pulse durations of less than 20 ns.

Capacitance[16]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{DD} = V_{DDQ} = 3.3V	TBD	pF
C_{CLK}	Clock Input Capacitance		TBD	pF
$C_{I/O}$	Input/Output Capacitance		TBD	pF

AC Test Loads and Waveforms



Thermal Resistance[16]

Parameter	Description	Test Conditions	BGA Typ.	TQFP Typ.	Units
Q_{JA}	Thermal Resistance (Junction to Ambient)	Still Air, soldered on a 4.25 × 1.125 inch, four-layer printed circuit board	TBD	TBD	°C/W
Q_{JC}	Thermal Resistance (Junction to Case)		TBD	TBD	°C/W

Switching Characteristics (Over the Operating Range)

Parameter	Description	-250		-200		-167		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Clock								
t_{CYC}	Clock Cycle Time	4.0		5		6		ns
F_{MAX}	Maximum Operating Frequency		250		200		167	MHz
t_{CH}	Clock HIGH	1.7		2.0		2.2		ns
t_{CL}	Clock LOW	1.7		2.0		2.2		ns
Output Times								
t_{CO}	Data Output Valid After CLK Rise		2.6		3.0		3.4	ns
t_{EOV}	$\overline{OE}$ LOW to Output Valid[16, 18, 20]		2.6		3.0		3.4	ns
t_{DOH}	Data Output Hold After CLK Rise	1.0		1.3		1.5		ns
t_{CHZ}	Clock to High-Z[16, 17, 18, 19, 20]		2.6		3.0		3.4	ns
t_{CLZ}	Clock to Low-Z[16, 17, 18, 19, 20]	1.0		1.3		1.5		ns
t_{EOHZ}	$\overline{OE}$ HIGH to Output High-Z[17, 18, 20]		2.6		3.0		3.4	ns
t_{EOLZ}	$\overline{OE}$ LOW to Output Low-Z[17, 18, 20]	0		0		0		ns
Set-up Times								
t_{AS}	Address Set-up Before CLK Rise					1.5		ns
t_{DS}	Data Input Set-up Before CLK Rise	1.2		1.4		1.5		ns
t_{CENS}	$\overline{CEN}$ Set-Up Before CLK Rise	1.2		1.4		1.5		ns
t_{WES}	$\overline{WE}$, $\overline{BWS_x}$ Set-up Before CLK Rise	1.2		1.4		1.5		ns

Notes:

15. Input waveform should have a slew rate of 2V/ns.
16. Tested initially and after any design or process change that may affect these parameters.
17. Unless otherwise noted, test conditions assume signal transition time of 1.5ns, timing reference levels of 1.5V, input pulse levels of 0 to 3.3V, and output loading of the specified I_{OL}/I_{OH} and load capacitance. Shown in (a), (b) and (c) of AC Test Loads.
18. t_{CHZ}, t_{CLZ}, t_{OEV}, t_{EOLZ}, and t_{EOHZ} are specified with AC test conditions shown in part (a) of AC Test Loads. Transition is measured ± 200 mV from steady-state voltage.
19. At any given voltage and temperature, t_{EOHZ} is less than t_{EOLZ} and t_{CHZ} is less than t_{CLZ} to eliminate bus contention between SRAMs when sharing the same data bus. These specifications do not imply a bus contention condition, but reflect parameters guaranteed over worst case user conditions. Device is designed to achieve High-Z prior to Low-Z under the same system conditions.
20. This parameter is sampled and not 100% tested.

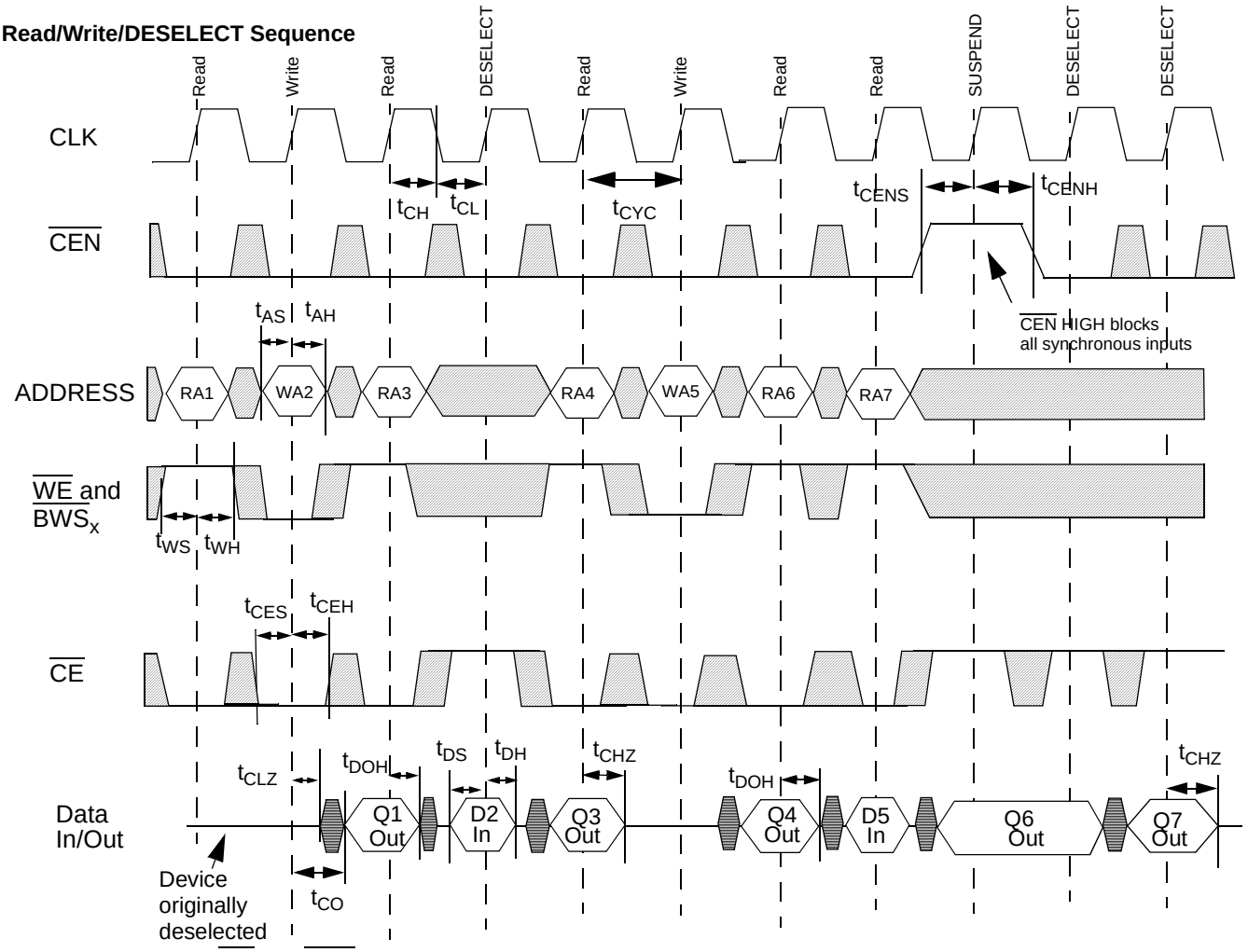
Switching Characteristics (Over the Operating Range) (continued)

Parameter	Description	-250		-200		-167		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{ALS}	ADV/$\overline{LD}$ Set-up Before CLK Rise	1.2		1.4		1.5		ns
t_{CES}	Chip Select Set-up	1.2		1.4		1.5		ns
Hold Times								
t_{AH}	Address Hold After CLK Rise	0.3		0.4		0.5		ns
t_{DH}	Data Input Hold After CLK Rise	0.3		0.4		0.5		ns
t_{CENH}	$\overline{CEN}$ Hold After CLK Rise	0.3		0.4		0.5		ns
t_{WEH}	$\overline{WE}$, $\overline{BW_x}$ Hold After CLK Rise	0.3		0.4		0.5		ns
t_{ALH}	ADV/$\overline{LD}$ Hold after CLK Rise	0.3		0.4		0.5		ns
t_{CEH}	Chip Select Hold After CLK Rise	0.3		0.4		0.5		ns

Shaded area contains advanced information.

Switching Waveforms

Read/Write/DESELECT Sequence

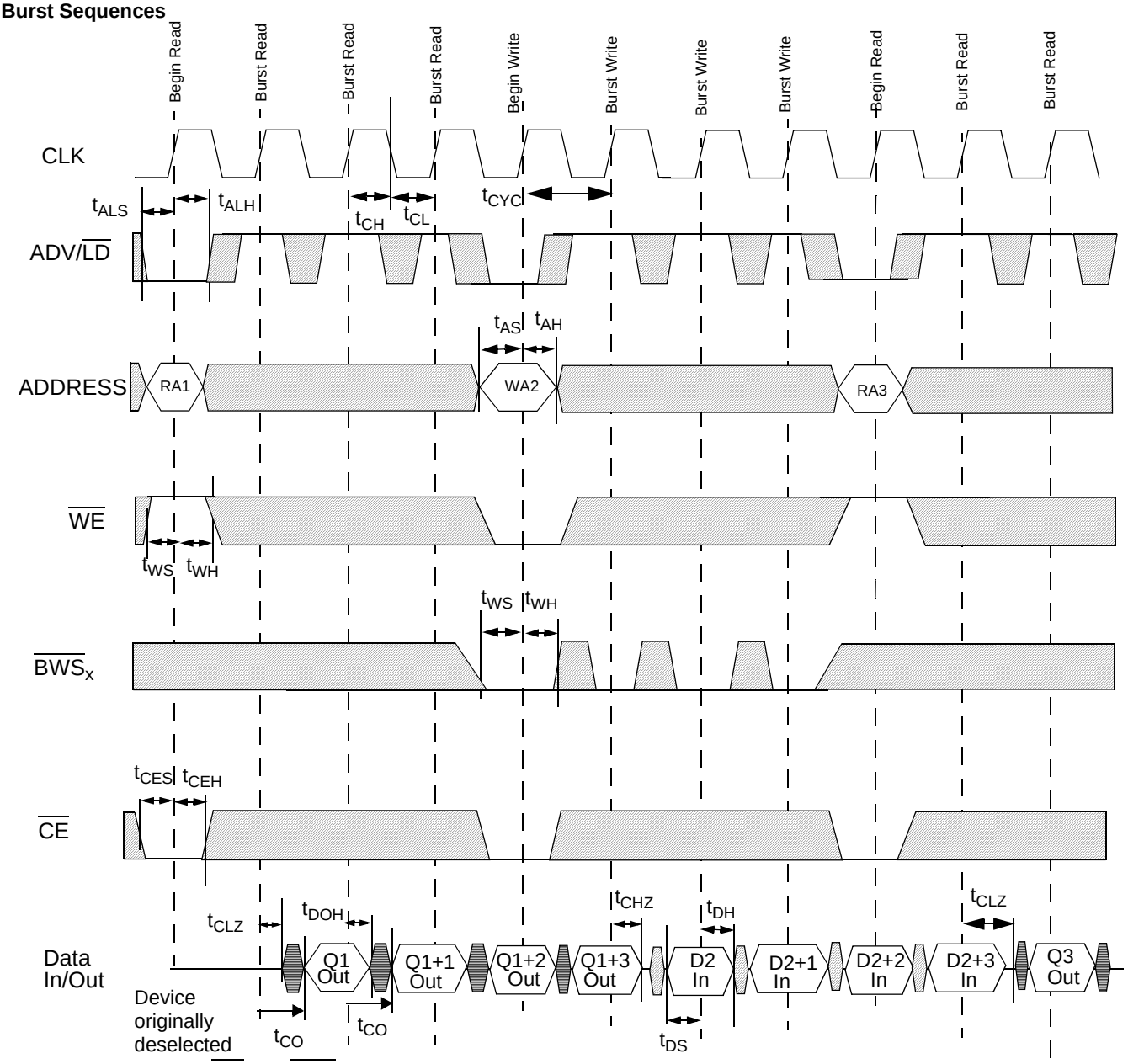


The combination of $\overline{WE}$ and $\overline{BWS_x}$ (x = a, b, c, d, e, f, g, h for x72, x = a, b, c, d for x36 and x = a, b for x18) defines a write cycle (see Write Cycle Description table). $\overline{CE}$ is the combination of $\overline{CE_1}$, CE_2, and $\overline{CE_3}$. All chip enables need to be active in order to select the device. Any chip enable can deselect the device. RAx stands for Read Address X, WAx stands for Write Address X, Dx stands for Data-in for location X, Qx stands for Data-out for location X. ADV/LD held LOW. OE held LOW.

= DON'T CARE = UNDEFINED

Switching Waveforms (continued)

Burst Sequences

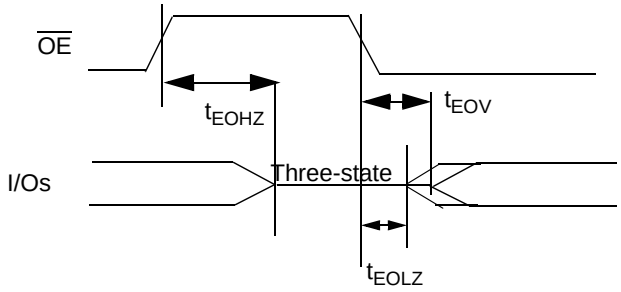


The combination of $\overline{WE}$ and $\overline{BWS_x}$(x = a, b, c, d, e, f, g, h for x72, x = a, b, c, d for x36 and x = a, b for x18) define a write cycle (see Write Cycle Description table). $\overline{CE}$ is the combination of $\overline{CE_1}$, CE_2, and $\overline{CE_3}$. All chip enables need to be active in order to select the device. Any chip enable can deselect the device. RAx stands for Read Address X, WA stands for Write Address X, Dx stands for Data-in for location X, Qx stands for Data-out for location X. $\overline{CEN}$ held LOW. During burst writes, byte writes can be conducted by asserting the appropriate $\overline{BWS_x}$ input signals. Burst order determined by the state of the MODE input. $\overline{CEN}$ held LOW. $\overline{OE}$ held LOW.

= DON'T CARE = UNDEFINED

Switching Waveforms (continued)

$\overline{OE}$ Timing



Ordering Information

Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
250	CY7C1470V33-250AC CY7C1472V33-250AC	A101	100-lead 14 × 20 × 1.4 mm Thin Quad Flat Pack	Commercial
	CY7C1470V33-250BGC CY7C1472V33-250BGC	BG119	119-ball BGA (14 × 22 × 2.4 mm)	
	CY7C1470V33-250BZC CY7C1472V33-250BZC	BB165C	165-ball FBGA (15 × 17 mm)	
	CY7C1474V33-250BGC	BG209	209-ball BGA (14 × 22 × 2.2 mm)	
200	CY7C1470V33-200AC CY7C1472V33-200AC	A101	100-lead 14 × 20 × 1.4 mm Thin Quad Flat Pack	
	CY7C1470V33-200BGC CY7C1472V33-200BGC	BG119	119-ball BGA (14 × 22 × 2.4 mm)	
	CY7C1470V33-200BZC CY7C1472V33-200BZC	BB165C	165-ball FBGA (15 × 17 mm)	
	CY7C1474V33-200BGC	BG209	209-ball BGA (14 × 22 × 2.2 mm)	
167	CY7C1470V33-167AC CY7C1472V33-167AC	A101	100-lead 14 × 20 × 1.4 mm Thin Quad Flat Pack	
	CY7C1470V33-167BGC CY7C1472V33-167BGC	BG119	119-ball BGA (14 × 22 × 2.4 mm)	
	CY7C1470V33-167BZC CY7C1472V33-167BZC	BB165C	165-ball FBGA (15 × 17 mm)	
	CY7C1474V33-167BGC	BG209	209-ball BGA (14 × 22 × 2.2 mm)	

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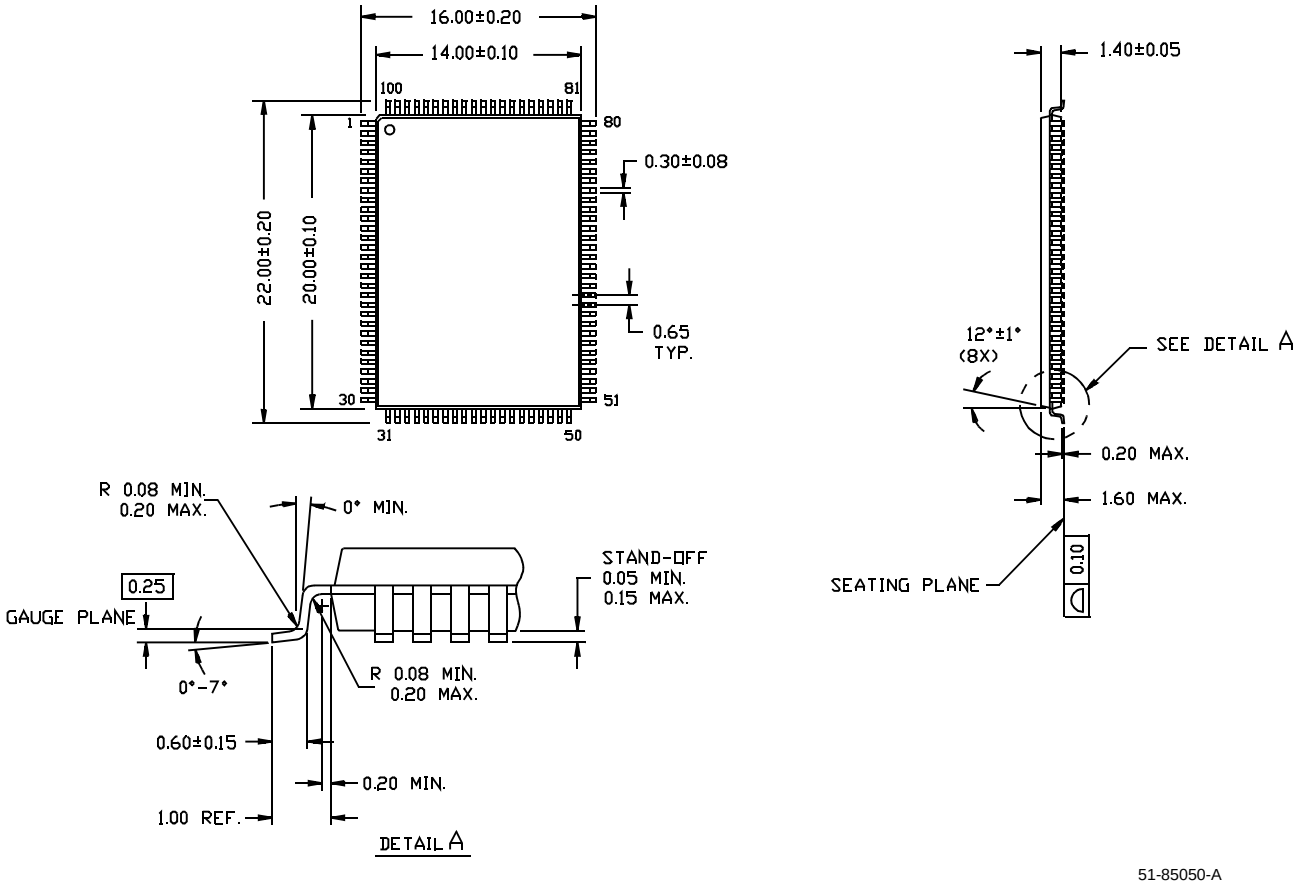
Package Diagrams

100-pin Thin Plastic Quad Flatpack (14 x 20 x 1.4 mm) A101

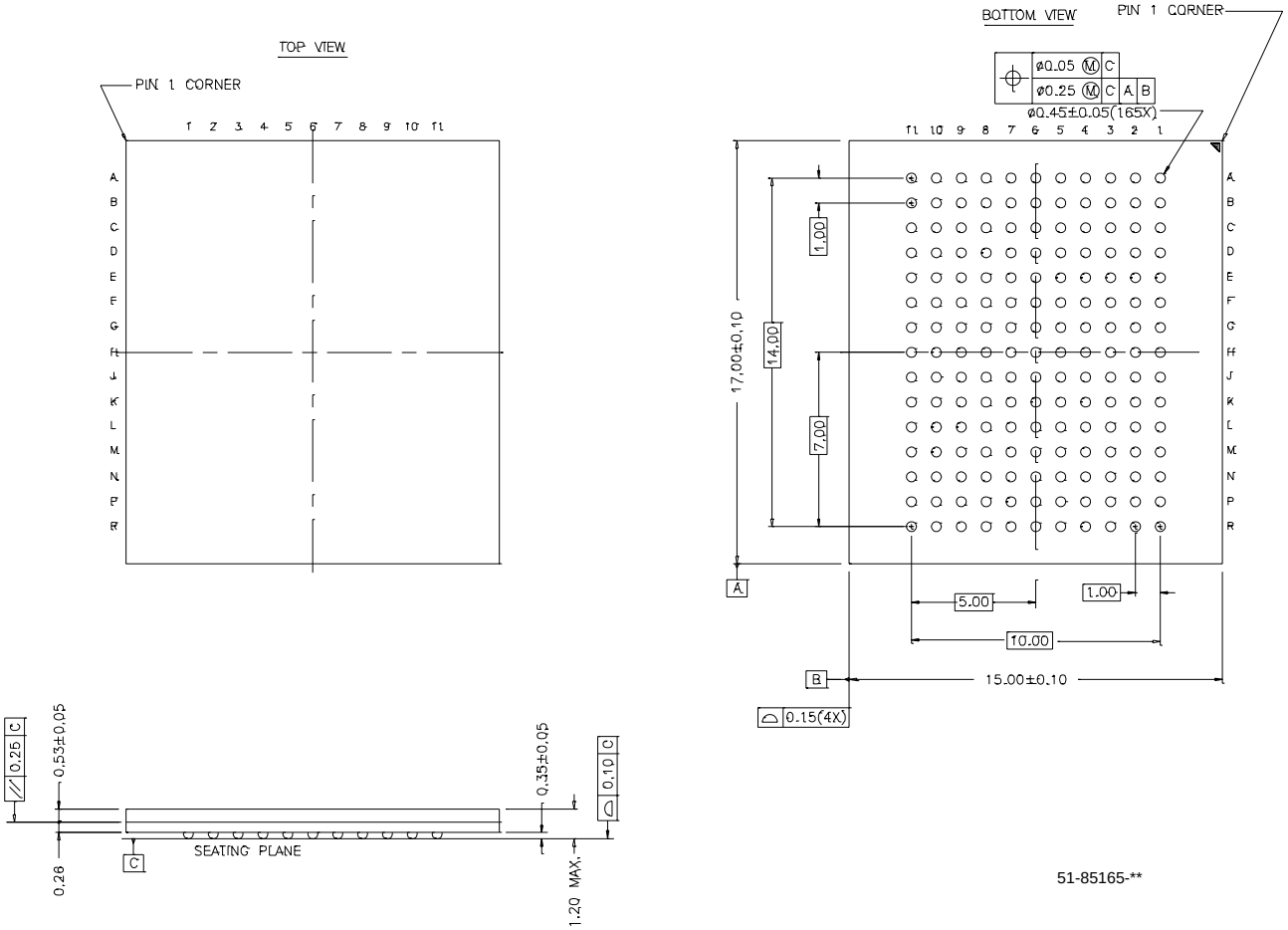
DIMENSIONS ARE IN MILLIMETERS.



51-85050-A

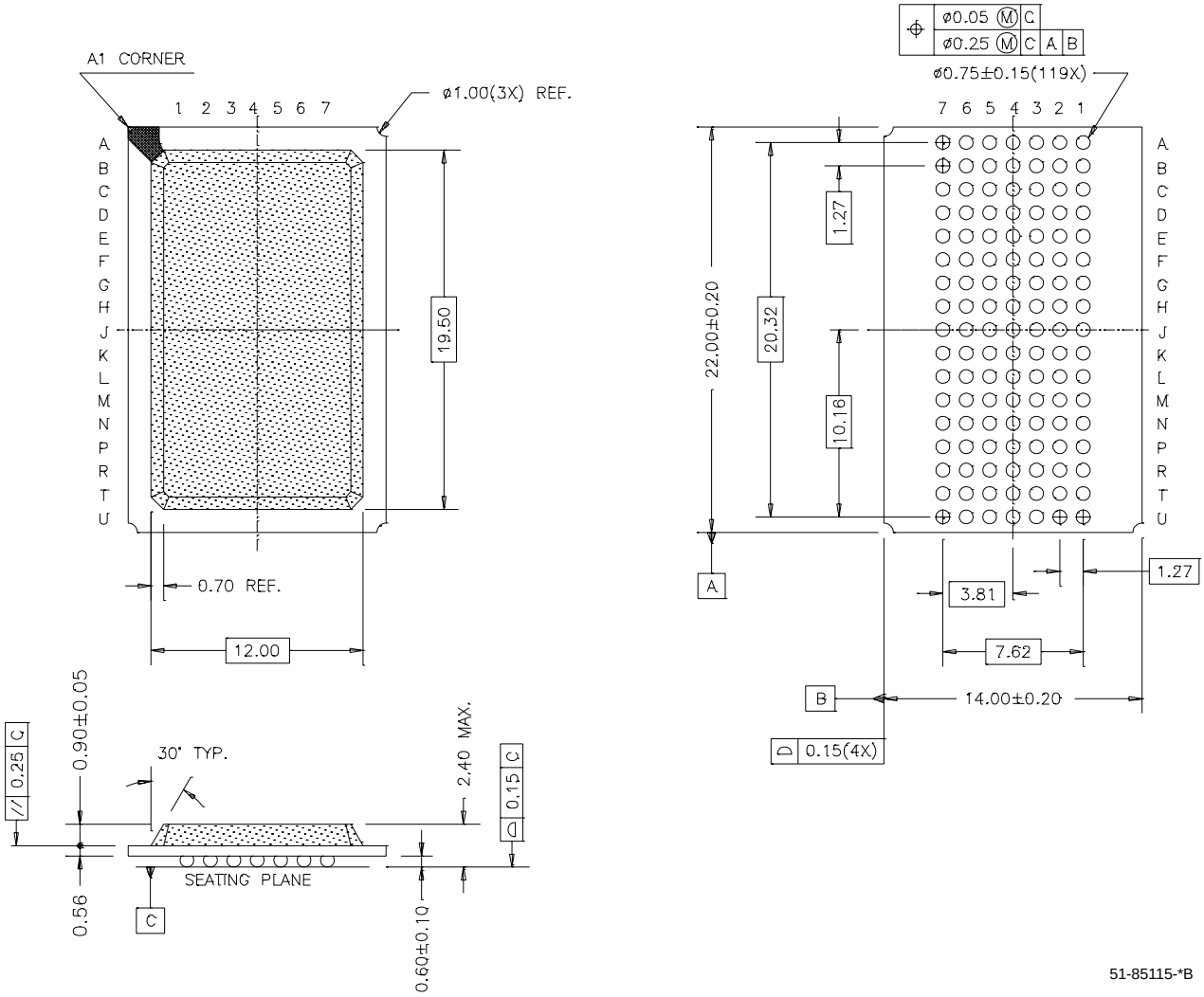
Package Diagrams (continued)

165-ball FBGA (15 × 17 × 1.20 mm) BB165C



Package Diagrams (continued)

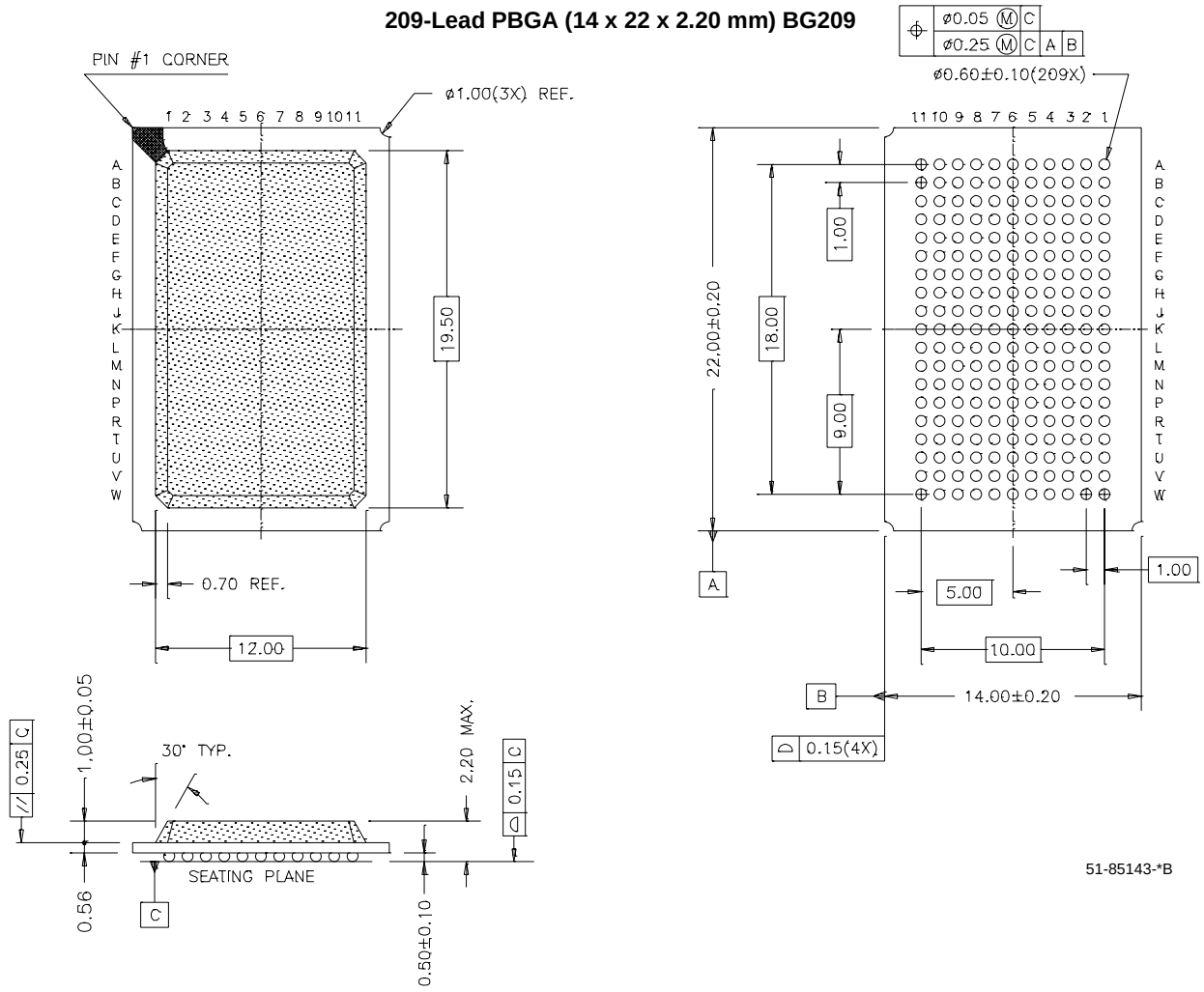
119-Lead PBGA (14 x 22 x 2.4 mm) BG119



51-85115-*B

Package Diagrams (continued)

209-Lead PBGA (14 x 22 x 2.20 mm) BG209



Document History Page

Document Title: CY7C1470V33/CY7C1472V33/CY7C1474V33 2M x 36/4M x 18/1M x 72 Pipelined SRAM with NoBL™ Architecture Document Number: 38-05289				
REV.	**ECN NO.**	**ISSUE DATE**	**ORIG. OF CHANGE**	**DESCRIPTION OF CHANGE**
**	114676	08/06/02	PKS	New Data Sheet
*A	121520	01/27/03	CJM	Updated features for package offering Removed 300MHz offering Changed tCO, tEOV, tCHZ, tEOHZ from 2.4 ns to 2.6 ns (250 MHz), tDOH, tCLZ from 0.8 ns to 1.0 ns (250 MHz), tDOH, tCLZ from 1.0 ns to 1.3 ns (200 MHz) Updated ordering information Changed Advanced Information to Preliminary